CALL FOR PAPERS

The Leading International Components, Packaging, and Manufacturing Technology Symposium

14th IEEE CPMT Symposium Japan

November 12 – 14, 2025
Venue: Ritsumeikan University Suzaku Campus, Kyoto, JAPAN
(On-site only)
https://www.ieee-csj.org

"Advanced Electronics Packaging Technology for Digital Twin"

"IEEE CPMT Symposium Japan (ICSJ)" is one of the most widely recognized international conferences sponsored by the **IEEE Electronics Packaging Society (EPS)** and is held annually in Kyoto every November. This conference was inaugurated in 1992 as "The VLSI Packaging Workshop in Japan (VPWJ)" to provide a platform to communicate and interact with global leaders in packaging technology. Later in 2010, this conference was renamed to "ICSJ," and ICSJ2025 is the 14th ICSJ meeting, or 23rd conference since establishing VPWJ.

Advanced Electronics Packaging Technology for Digital Twin: A digital twin is a set of adaptive digital models of a real-world complex system, which acts as a virtual counterpart or "twin", which enables advanced monitoring and forecasting of that system by performing physical simulations that are as close to reality as possible based on a huge amount of data collected in real time. Crucially using a large parameter set it also enables complex test operations to show how a real system will respond to a variety of different scenarios.

Digital twin technology is already being applied in different industrial fields, such as automated driving, robotic control and medicine. The core technologies that support the digital twin include IoT, AI/ML, B5G, and AR/VR. Specifically, these technologies are comprised of sensor technologies that collect data from the real world, information and communication networks that transmit data with high bandwidth and low latency; and advanced electronic devices technology that perform data analysis, computation, simulation, machine learning, and deep learning. As the use cases of the digital twin increases opportunities, advanced semiconductor devices (including edge computing devices), sensor devices, and relating to interconnect technology will become increasingly important as the foundation for the digital twin in order to enable low latency, high bandwidth, and low power consumption. In 2025, our focus is on key electronics packaging technologies for digital twin and emphasizes the following main topics: **Photonics, Advanced Packaging & Emerging Technologies, Power & Automotive Electronics, Process & Material, Signal/Power Integrity** and **Bioelectronics & Healthcare**. Additional topics of primary interest to the participants are listed below.

Other topics include (but not limited to):

+ 2.xD & 3D package for chiplets
+ Fine pitch assembly & hybrid bonding
+ Materials & processing for panel level package
+ Co-packaged Optics (CPO) & materials for optical packaging
+ Packaging for high-speed electronic interconnect
+ Packaging for neuromorphic or quantum computing
+ Resilient packaging for autonomous systems
+ Packaging for sensor & MEMS devices
+ Signal integrity & power integrity
+ RF components & modules
+ Low power, low temperature & ultra-low noise system packaging

This conference will be a perfect opportunity to communicate, interact, exchange technical ideas, and discuss your latest novel research findings in packaging technologies with experts from industry and academia. In addition to the regular sessions, there is an “Early Career Researchers’ (ECR)” session for young researchers with less than two year’s experience in their professions and all students including Ph.D. to hold fruitful discussions with the experts. The ECR sessions will be held as a poster session. Authors are invited to submit an abstract through our website https://www.ieee-csj.org. **The abstract deadline is extended on June 13, 2025**. Notification of acceptance will be sent by July 4, 2025, and the successful authors would then be requested to submit a 4-page manuscript by September 4, 2025, for the Technical Digest, which will be available via **IEEE Xplore Digital Library**, while the authors for the ECR session are required to submit a 2-page manuscript.

ICSJ2025 Steering Committee:

General Chair	Hideyuki Nawata	(Nissan Chemical Corporation)
Vice Chair	Yutaka Uematsu	(Hitachi, Ltd.)
	Kitty Pearsall	(Boss Precision Inc.)
Program Chair	Kazuyuki Nakagawa	(Renesas Electronics Corporation)
	Kenji Takahashi	(AIST)
	Takafumi Fukushima	(Tohoku University)
Conference Relations Chair	Shinya Takyu	(LINTEC Corporation)
	Eiji Higurashi	(Tohoku University)
Promotion Chair	Takaaki Ishigure	(Keio University)
	Hideyuki Nasu	(Furukawa Electric Co., Ltd.)
	Taiji Sakai	(TSMC Japan 3DIC R&D Center, Inc.)
Financial Chair	Hidetoshi Numata	(IBM Research - Tokyo)
	Satomi Kawamoto	(Namics Corporation)
	Jun Maeda	(LINTEC Corporation)
Sponsor-Care Chair	Tadatomo Yamada	(LINTEC Corporation)
	Wataru Shiroi	(Renesas Electronics Corporation)
Publication/Web Chair	Junichi Inoue	(Kyoto Institute of Technology)
	Chinami Marushima	(IBM Japan, Ltd.)
Arrangement Chair	Takashi Hare	(Toray Engineering Co., Ltd.)
	Kentaro Kaneko	(Ritsumeikan University)
	Kai Takeuchi	(Tohoku University)
	Kazutaka Maeda	(KYOCERA Corporation)
	Yuta Sugawara	(KYOCERA Corporation)

Financial Sponsor:
IEEE Electronics Packaging Society (EPS)
Technical Co-Sponsor:
IEEE EPS Japan Chapter

On-site Conference Venue:
Ritsumeikan University Suzaku Campus
Nishinokyosuzakucho 1, Nakagyoku, Kyoto, 604-8520